NATIONAL UNIVERSITY OF SINGAPORE

School of Computing

C S S E M I N A R

Title: **Energy Aware Network Computing: Packet Processing with Multicore Processors**

Speaker: Distinguished Professor Laxmi Narayan Bhuyan
Department of Computer Science and Engineering
University of California, Riverside (UCR)

Date/Time: 28 July 2016, Thursday, 02:00 PM to 03:30 PM

Venue: Executive Classroom, COM2-04-02

Chaired by: Dr Mitra, Tulika, Professor, School of Computing
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Abstract:

Network computing is the execution of various applications at servers, routers and end points in the Internet by processing packets on the fly. Unlike scientific computing, it is characterized by a request arrival process at the server, intermittent service demands, customized computations, and departures. The applications include web service, data center workloads, content aware routing, deep packet inspection (DPI), and multimedia, etc. The processing can be computationally expensive that adds delays, reduces throughput, and degrades the quality of service (QoS) of the requests. Also, energy saving in network equipment and servers has assumed paramount importance in recent times. This talk presents different techniques that can be adopted to save power and energy consumption in multicore packet processing.

Our research over the years has developed techniques to tackle the problems of packet processing by designing efficient scheduling techniques for multicore architectures. By exploiting locality and load balancing at the same time, we have developed and tested different algorithms on commercial platforms for many applications. In addition to presenting brief results on scheduling, this presentation will focus on different techniques to save energy in a multicore server. We develop suitable load distribution of incoming packets to multiple cores in the server, and apply DVFS and clock gating power saving techniques. Our research also develops vacation and rate adaptation schemes and saves power by driving the CPU cores to deep sleep states. At the same time, latency and QoS are considered so as not to violate their constraints. Both static and runtime techniques are designed, implemented, and evaluated using commercial multicore processors. Some measurement results are presented.

Biodata:

Laxmi Narayan Bhuyan is Distinguished Professor of Computer Science and Engineering Department at the University of California, Riverside (UCR). Prior to joining UCR, he was a professor of Computer Science at Texas A&M University and Program Director of the Computer System Architecture Program at the National Science Foundation. His current research interests are in the areas of network packet processing, multiprocessor architectures, heterogeneous architectures, parallel and distributed processing, and performance evaluation. He has been named as an ISI Highly Cited Researcher in Computer Science. Dr. Bhuyan served as the Editor-in-Chief of the IEEE Transactions on Parallel and Distributed Systems (TPDS) from 2006-2009 and was the founding Program Committee Chairman of the HPCA in 1995. Dr. Bhuyan is a Fellow of the IEEE, a Fellow of the ACM, a Fellow of the AAAS (American Association for the Advancement of Science), and a Fellow of the WIF (World Innovation Foundation).

For more information on his research and professional activities, please visit http://www.cs.ucr.edu/~bhuyan/