NATIONAL UNIVERSITY OF SINGAPORE

School of Computing

PH.D DEFENCE - PUBLIC SEMINAR

Title: **Efficient Power Management for Heterogeneous Multi-Core Architectures**

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Abstract:

Relentless Complementary Metal-Oxide Semiconductor (CMOS) scaling at deep sub-micron level has resulted
in increased power density in microprocessor, which forced the computing systems to move in the direction of parallel architectures with homogeneous multi-cores. However, the emergence of dynamic and diverse workloads combined with the failure of Dennard Scaling facilitated the growth of heterogeneous multi-cores. The presence of heterogeneity enables better match between application demand and computation capabilities leading to substantially improved performance and energy-efficiency. In spite of significant benefits in terms of both performance and energy consumption, the heterogeneous multi-core systems introduce many of design and scheduling challenges. In this thesis, we address various challenges involved in designing heterogeneous multi-cores.

In the first part of this thesis, we focus on developing power management schemes for heterogeneous multi-cores that can satisfy application?s demand with low energy consumption under the Thermal Design Power (TDP) constraint. First, we develop a performance and power model of heterogeneous cores having different performance and power consumption characteristics that can be used in any predictive scheduling approach. Second, we propose two reactive power management frameworks: Hierarchical Power Management (HPM) and Price theory based Power Management (PPM). All the aforementioned dynamic power management frameworks were evaluated on a real Advance RISC Machines (ARM) big.LITTLE heterogeneous multi-core platform. Our experimental evaluations establish the superiority of the power management schemes compared to the existing state-of-the-art techniques. Lastly, we propose a power-aware dynamic reliability management technique that can meet both reliability and thermal/power constraints, while optimizing the performance.

In the second part of this thesis, we propose a comprehensive framework that help to design

the most energy-efficient application-specific Multi-Processor System on Chips (MPSoCs). We model the synthesis of energy-efficient MPSoC as a design space exploration problem involving four design parameters: DVFS, processor customization, cache customization and task mapping. Experiments reveal that our framework can reduce energy consumption compared to solutions obtained from a combination of existing techniques.

Overall in this thesis, we address power consumption related challenges exhibited in heterogeneous multi-core systems by proposing both static and dynamic power management techniques. While the first part of the thesis focuses on the dynamic techniques, the second part elaborates the static solutions.