## NATIONAL UNIVERSITY OF SINGAPORE School of Computing

## PH.D DEFENCE - PUBLIC SEMINAR

Title:	Techniques for Crafting Customizable MPSoCs
Speaker:	Mr Chen Liang
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## Abstract:

General-purpose processors offer high flexibility in terms of supporting wide range of applications, however, they hardly meet the high performance demands of computationally intensive applications. A common method for bridging the gap between flexibility and performance demands is to add customized accelerators into general-purpose processors. These customized accelerators are designed to explore the special features of different applications so that they can achieve dramatic speedups.

On the other hand, with the inevitable transition into the multi-core era, heterogeneity is emphasized to improve the overall efficiency of the application executions. Rather than integrating multiple simple cores within one chip, each of the cores could be tailored through customization techniques to meet the specific demands of the applications.

In this thesis, we investigate the issues for customizing multiprocessor system-on-chips (MPSoCs). Our objective is to propose a design automation toolchain for MPSoC customizations. The complete tool chain should cover the architectural designs, compiler supports and design space exploration techniques.

At the beginning, we take a step to create a heterogeneous MPSoC system statically by using custom functional units. The custom functional units are designed for accelerating different custom instruction sets. The total area for accommodating custom functional units is implicitly shared among the cores. The limited area budget and alternative customization choices present a challenging optimization problem for design space exploration. A dynamic programming algorithm is then designed to optimally retrieve the set of custom instructions for every task of the targeting application so as to have the highest speedup under the area constraint.

The customization problem becomes more challenging when reconfigurable fabric is adopted and shared among multiple cores. The first customization problem is the

architectural design. To come up with a concrete reconfigurable architecture, we propose a novel custom functional unit design that can be reconfigured to support most of the identified custom instructions across multiple application domains. The efficiency of the custom functional unit design is then evaluated by integrating it into the the pipeline to form a just-in-time reconfigurable processor. A coarse-grained reconfigurable array would be designed using the proposed custom functional unit as the primary processing element. By attaching the coarse-grained reconfigurable array with multiple cores, we come up with a concrete customizable MPSoC architecture.

We then study the second design automation problem, the compilation supports. We formulate the problem of mapping loop kernels onto the reconfigurable fabric as a graph minor containment problem. With the formalization, we design an efficient search algorithm adopted from the graph theory domain to solve the mapping problem. To further improve the efficiency of the application mapping, a pre-processing compilation step will be added to condense the executions of multiple operations.

Other than architectural design and compilation supports, the final problem in the design automation toolchain is the design space exploration. With the presence of a shared reconfigurable fabric, the complexity of the design space is dramatically increased comparing to the static approach. The problem is now not only how to choose the appropriate customization sets sharing the area of the fabric, but also making the decisions for when the reconfigurations should be conducted. We propose an optimal solution based on dynamic programming for this problem.