

# NATIONAL UNIVERSITY OF SINGAPORE

School of Computing

## PH.D DEFENCE - PUBLIC SEMINAR

**Title:**            **A Dynamic Heterogeneous Multi-Core Architecture**

Speaker:        Mr. Pricopi Mihai

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Venue:           Executive Classroom, COM2-04-02

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### Abstract:

Computing systems have made an irreversible transition towards parallel architectures with the emergence of multi-cores. The existing trends indicate that multi-cores (and even many-cores) will comprise of collections of simple cores rather than complex cores. However, contemporary applications have highly diverse computation requirements that are hard to satisfy with a set of simple homogeneous cores. While parallel applications can benefit from thread-level parallelism offered by such multi-core solutions, there still exist a large number of applications with substantial amount of sequential code. The sequential programs suffer from limited exploitation of instruction-level parallelism in the simple cores.

In this thesis, we design and evaluate a novel dynamic heterogeneous multi-core architecture, called Bahurupi, that can successfully reconcile the conflicting demands of instruction-level and thread-level parallelism. Bahurupi can accelerate the performance of serial code by dynamically forming coalition of two or more simple cores to offer increased instruction-level parallelism. In particular, Bahurupi can efficiently merge 2-4 simple 2-way out-of-order cores into coalition to reach or even surpass the performance of more complex and power-hungry 4-way or 8-way out-of-order core. Additionally, we introduce a novel reconfigurable L1 data cache architecture for Bahurupi that is able to accommodate the memory demands of a dynamic heterogeneous multi-core architecture with low area and energy overhead.

A fundamental challenge in exploiting dynamic heterogeneous multi-cores arises from appropriately scheduling the workload on such a flexible architecture design. We design offline and online schedulers that intelligently reconfigure and allocate the cores to a mix of sequential and parallel applications so as to minimize the overall makespan. Experimental evaluation confirms that dynamic heterogeneous multi-core architectures can substantially improve the performance compared to homogeneous and static heterogeneous multi-core architectures.